Digital Circuits

ECS 371

Dr. Prapun Suksompong

prapun@siit.tu.ac.th

Lecture 17

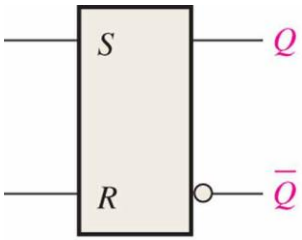
Office Hours:
BKD 3601-7
Monday 9:00-10:30, 1:30-3:30
Tuesday 10:30-11:30

ECS371.PRAPUN.COM

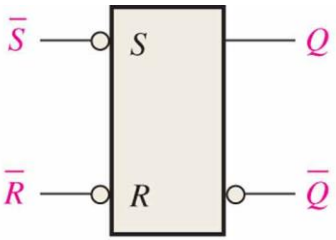
Announcement

- Reading Assignment:
  - Chapter 7: 7-1, 7-2, 7-4
- We will use the old handout from last time.

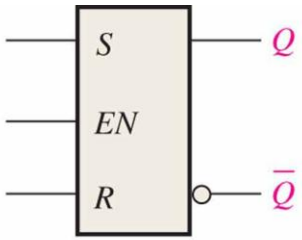
Logic Symbols: Latches and Flip-Flops



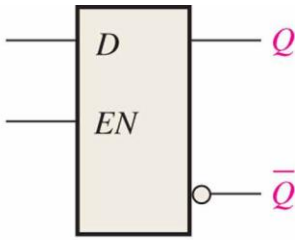
(a) Active-HIGH input S-R latch



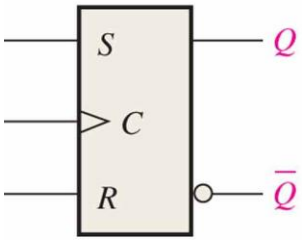
(b) Active-LOW input $\overline{S}$-$\overline{R}$ latch

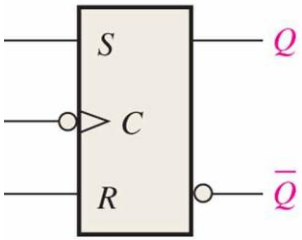


(c) Gated S-R latch

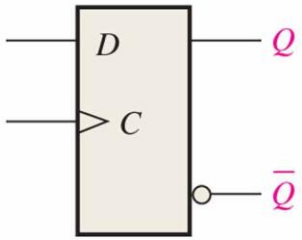


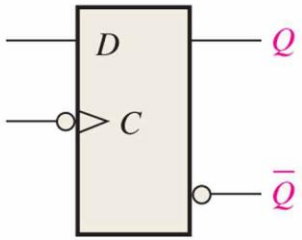
(d) Gated D latch



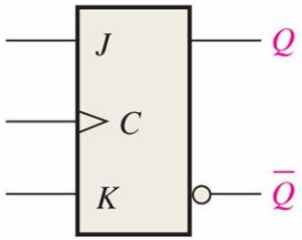


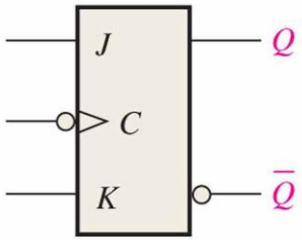
(e) S-R edge-triggered flip-flops





(f) D edge-triggered flip-flops

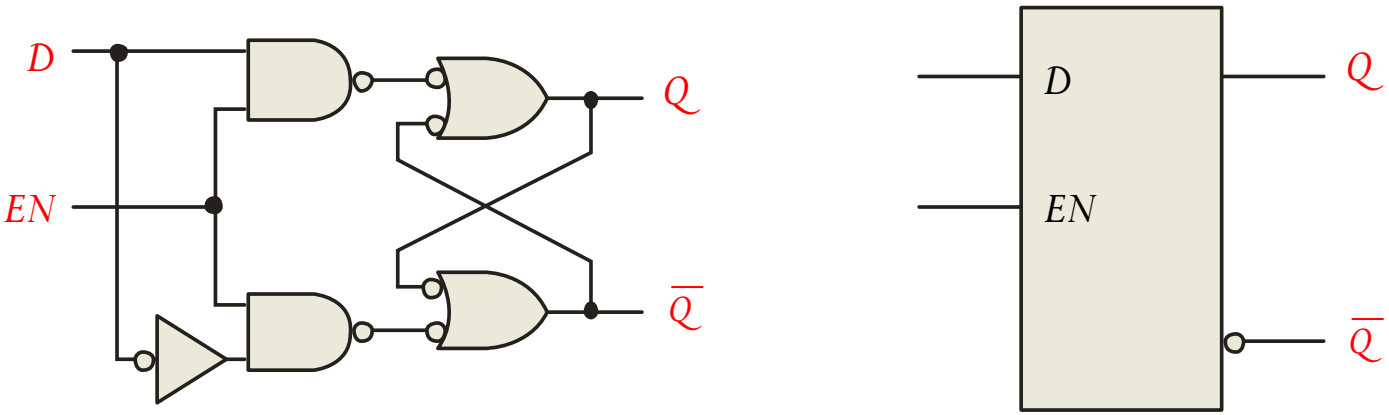




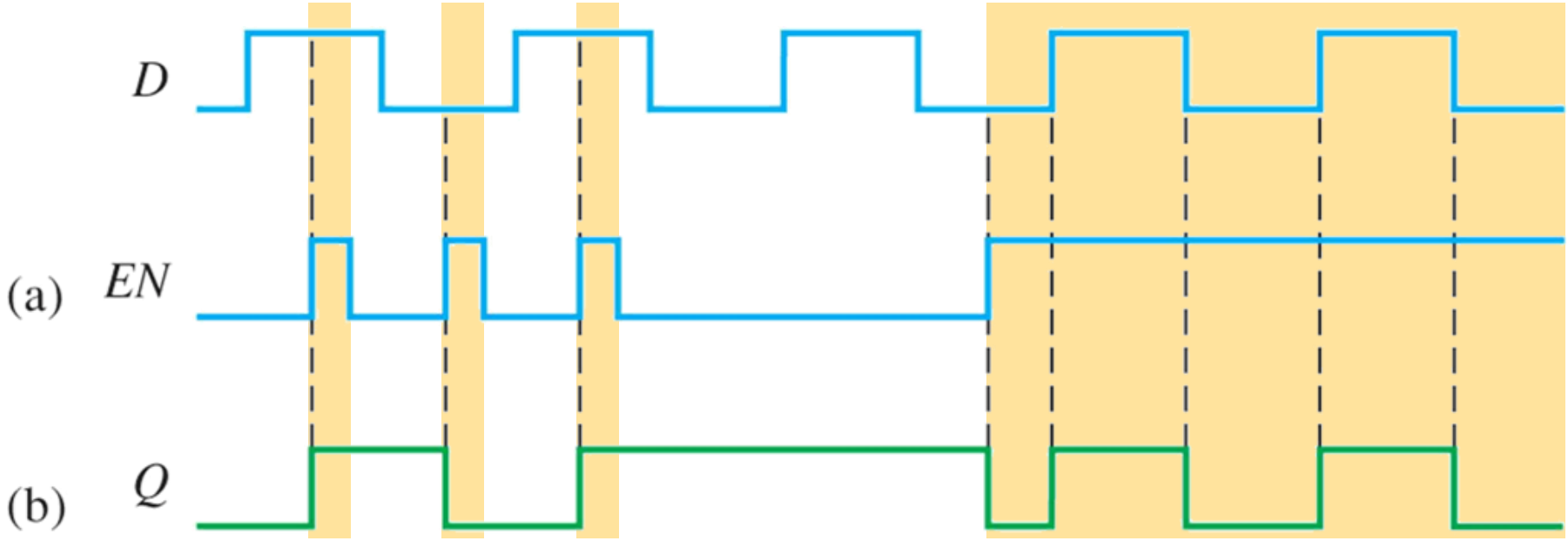
(g) J-K edge-triggered flip-flops

Gated D latch

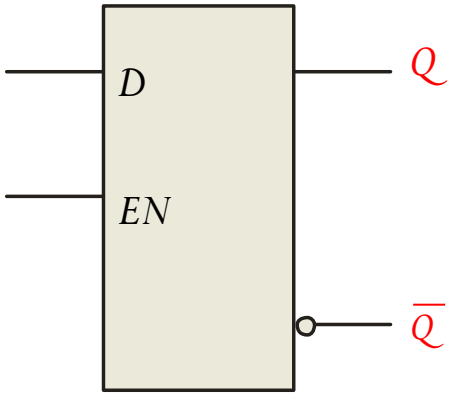
- The D latch is a variation of the S-R latch.
- Has only one input in addition to EN.
  - This input is called the D (data) input.
- Combine the S and R inputs into a single D input.



Example: Gated D Latch



Q follows D when the Enable is active.



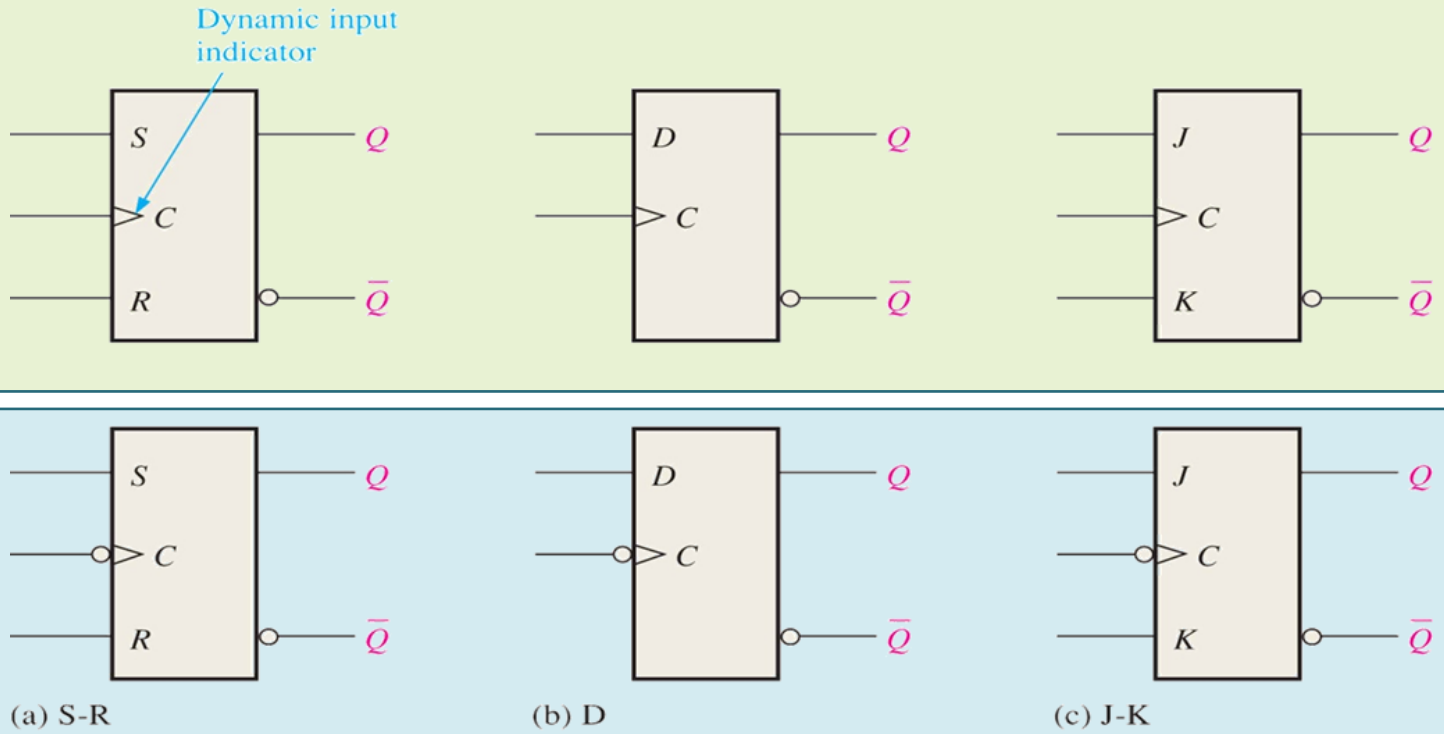
Flip-Flop

- Latches *sample* their inputs (and change states) *any time* the EN bit is asserted.
- Flip-flops are **synchronous**: the output changes state only at a specified point on the *triggering input* called the **clock (CLK)**
  - In other words, changes in the output occur in synchronization with the clock.
- An **edge-triggered flip-flop** changes state either at the **positive edge (rising edge)** or at the **negative edge (falling edge)** of the clock pulse.

Edge-Triggered Flip-Flops

"Edge-triggered flip-flop" is redundant (all flip-flops are edge-triggered

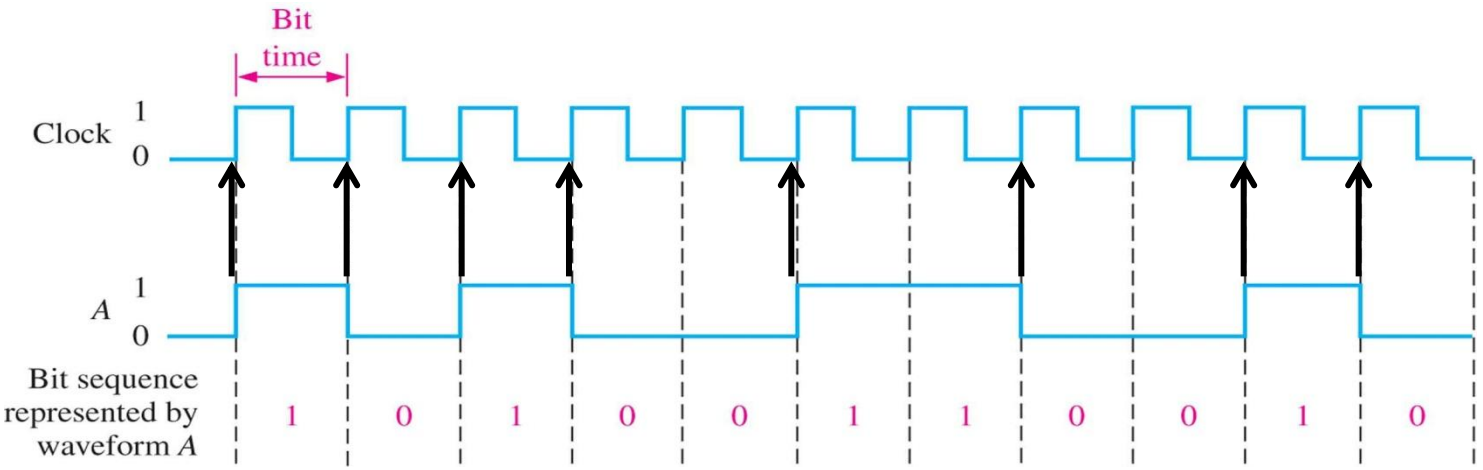
Positive edge-triggered (no bubble at C input)



Negative edge-triggered (bubble at C input)

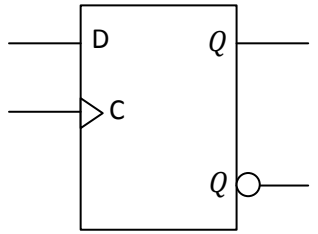
Clock (CLK)

- In digital synchronous systems, all waveforms are synchronized with a clock.
  - The clock waveform itself does not carry information.
- The **clock** is a periodic waveform in which each interval between pulses (the period) equals the time for one bit.



- Notice that change in level of waveform *A* occurs at the **rising edge** of the clock waveform.

D Flip-Flop



- The truth table for a positive-edge triggered D flip-flop shows an up arrow to remind you that it is sensitive to its D input only on the **rising edge of the clock**.
- The truth table for a negative-edge triggered D flip-flop is identical except for the direction of the arrow.

Inputs		Outputs		
D	CLK	*Q*	$\overline{Q}$	Comments
1	↑	1	0	SET
0	↑	0	1	RESET

(a) Positive-edge triggered

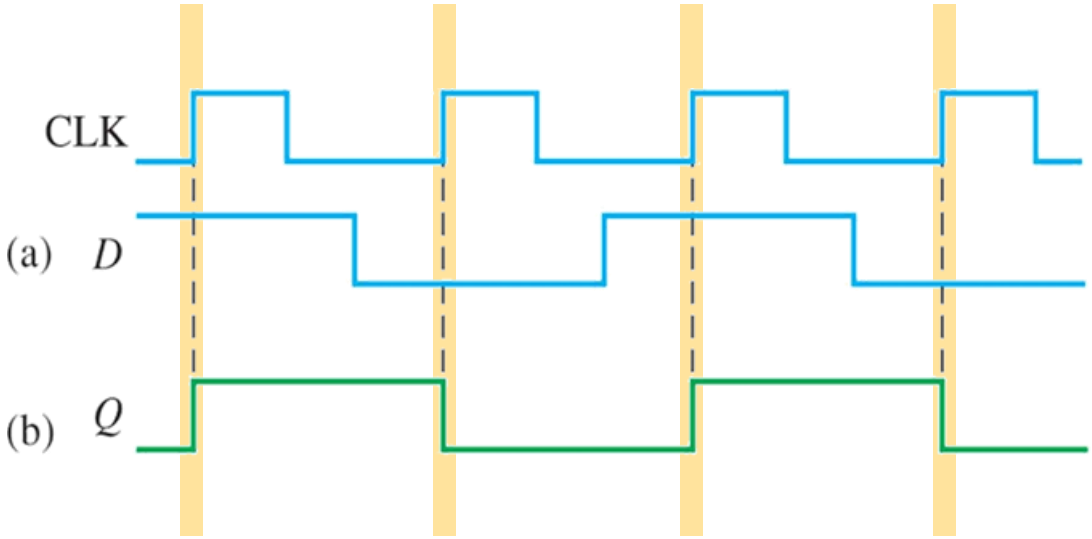
Inputs		Outputs		
D	CLK	*Q*	$\overline{Q}$	Comments
1	↓	1	0	SET
0	↓	0	1	RESET

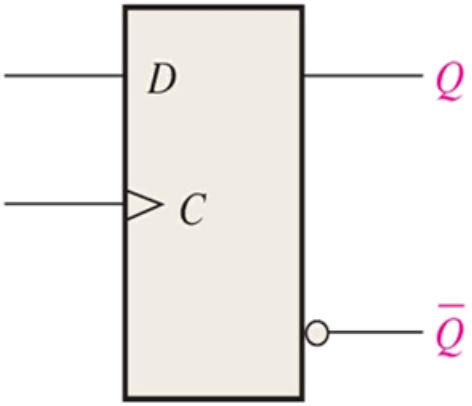
(b) Negative-edge triggered

↑= clock transition LOW to HIGH

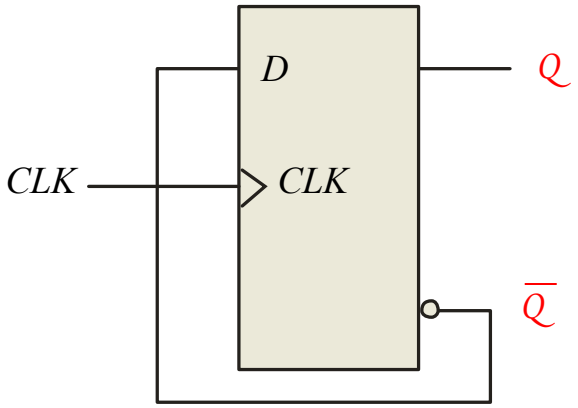
Ex: Positive-edge triggered D Flip-Flop

- Determine the Q output waveform if the flip-flop starts out RESET



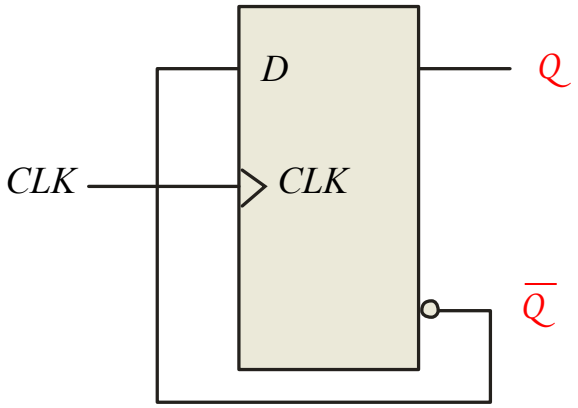


Exercise



What specific function does this device perform?

Exercise

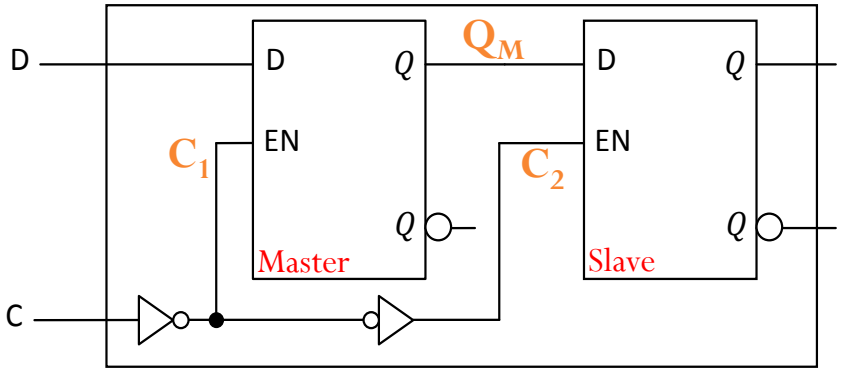


It is a D flip-flop hardwired for a **toggle mode**.

For example, if Q is LOW, $\overline{Q}$ is HIGH and the flip-flop will toggle on the next clock edge. Because the flip-flop only changes on the active edge, the output will only change once for each clock pulse.

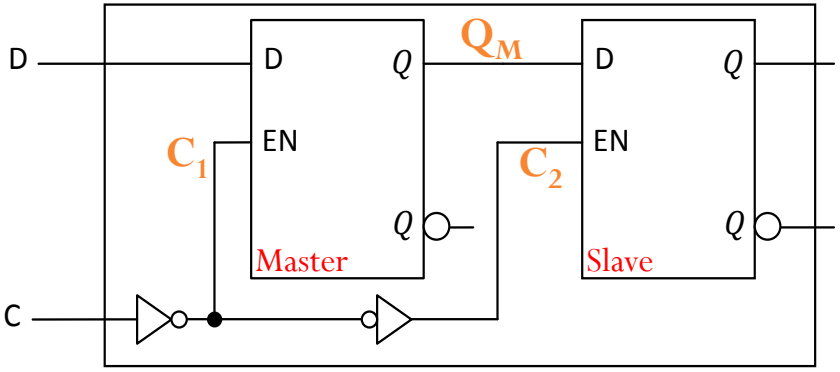
D Flip Flop: Implementation

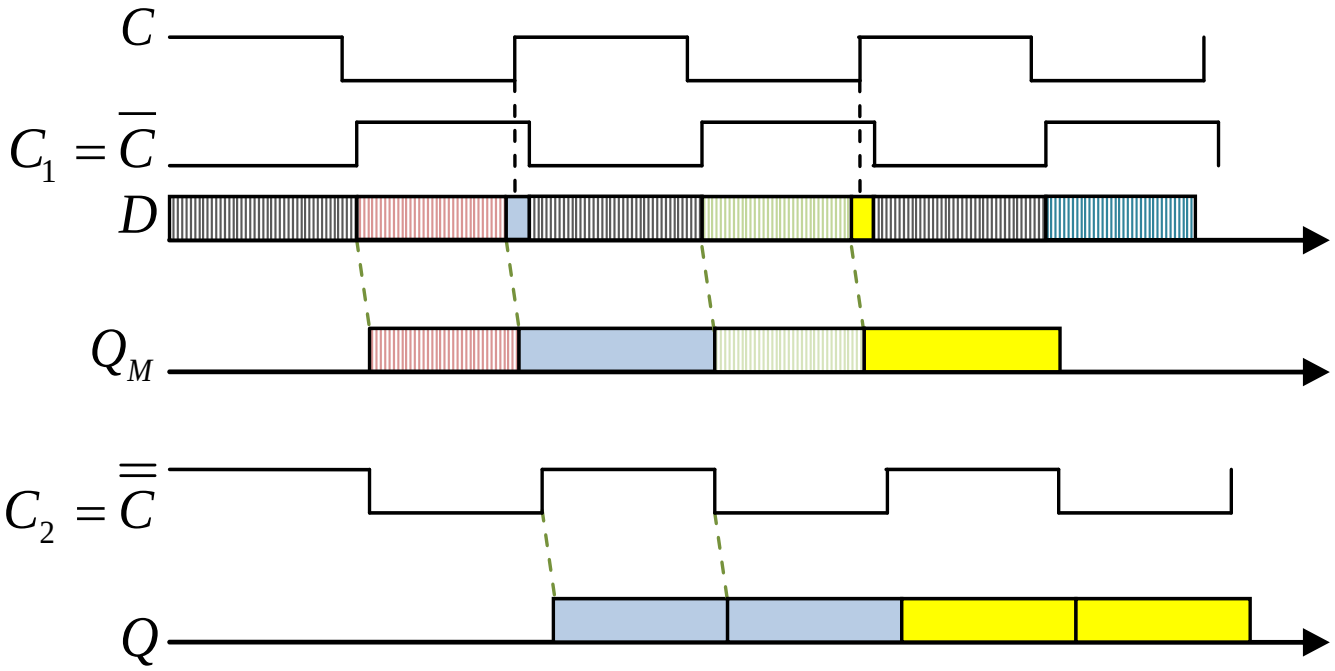
- Tie two D-latches together to make a D flip-flop



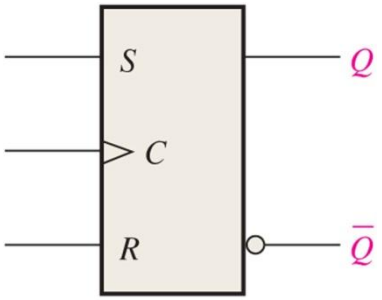
- When C is 0 ($C_1 = 1$), the master latch is open and follows the D input.
- When C is 1 ($C_1 = 0$, $C_2 = 1$), the master latch is closed and its output is transferred to the slave latch.
  - The slave latch is open all the while that C is 1, but changes only at the beginning of this interval, because the master is closed and unchanging during the rest of the interval.

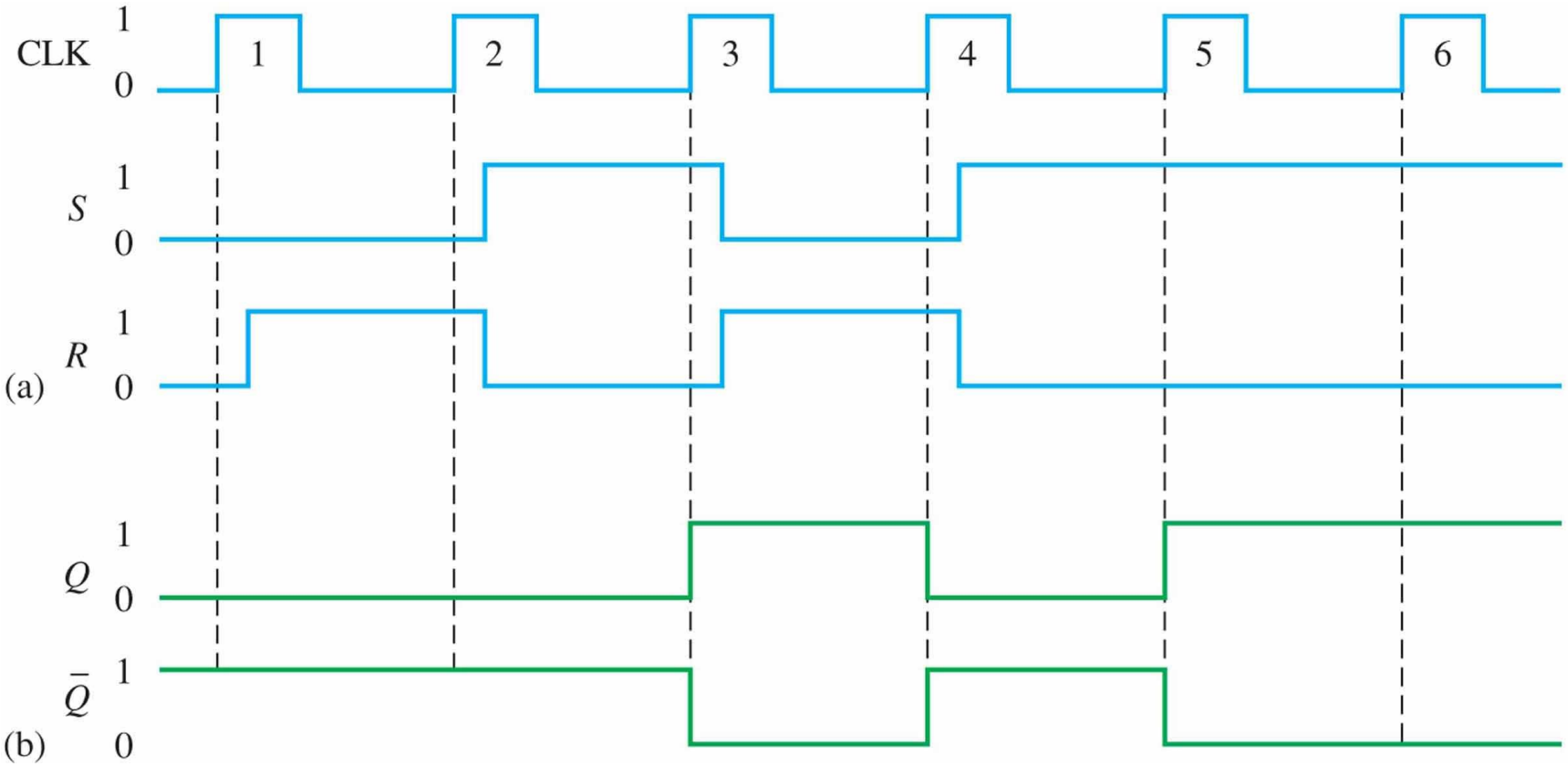
D Flip Flop: Implementation





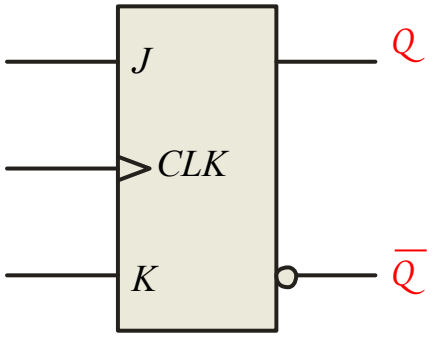
S-R Flip-Flop





J-K Flip-Flop

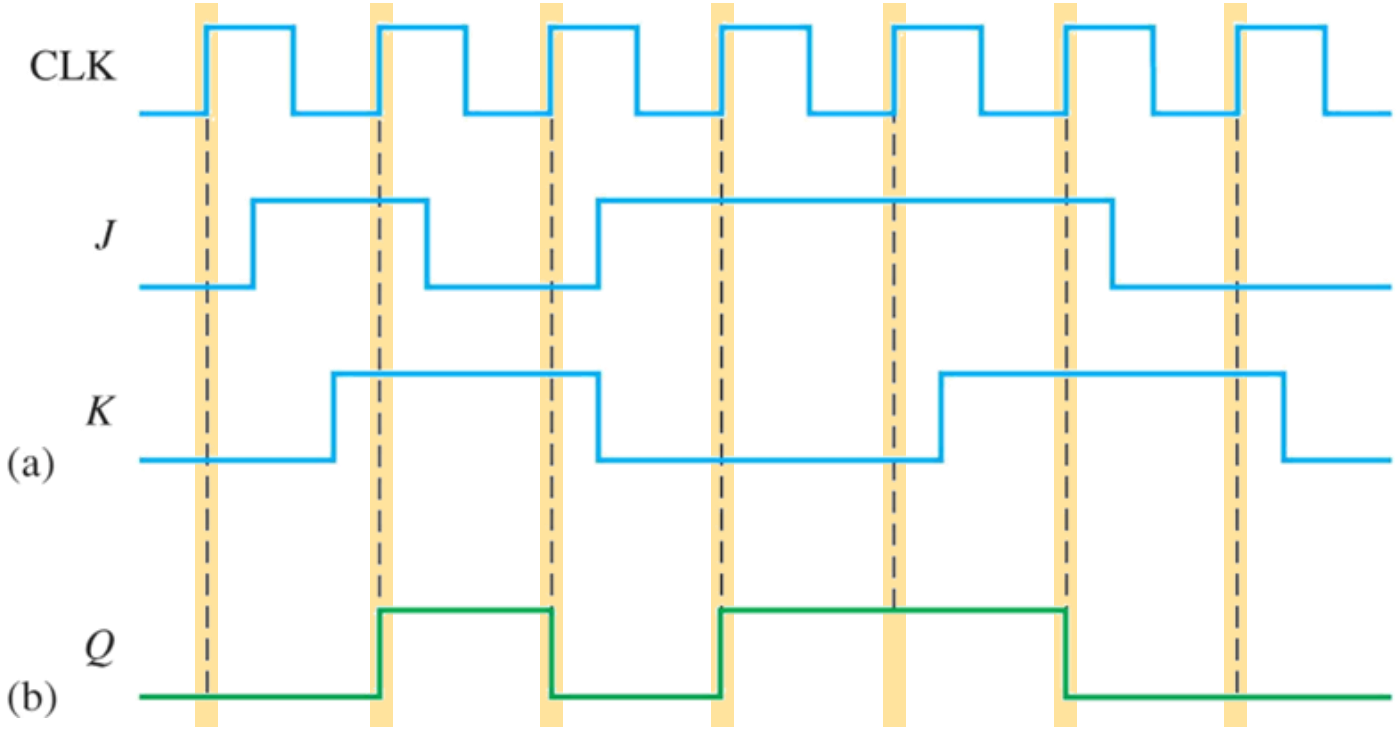
- Has two inputs, labeled J and K (along with the CLK).
- When both J and K = 1, the output changes states (toggles) on the rising clock edge.

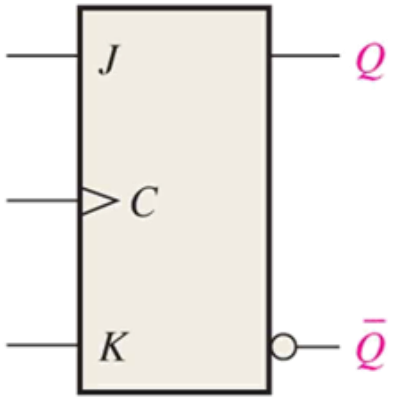


Inputs			Outputs		
J	*K*	CLK	*Q*	$\overline{Q}$	Comments
0	0	↑	Q_0	$\overline{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	$\overline{Q}_0$	Q_0	Toggle

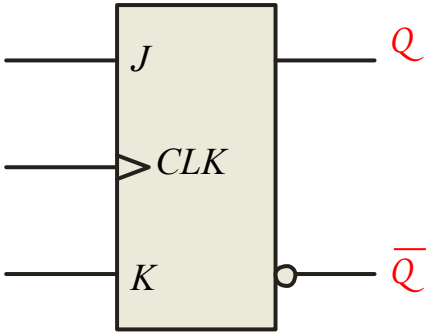
A J-K flip-flop connected for toggle operation is sometimes called a **T flip-flop**.

Example: J-K Flip-Flop

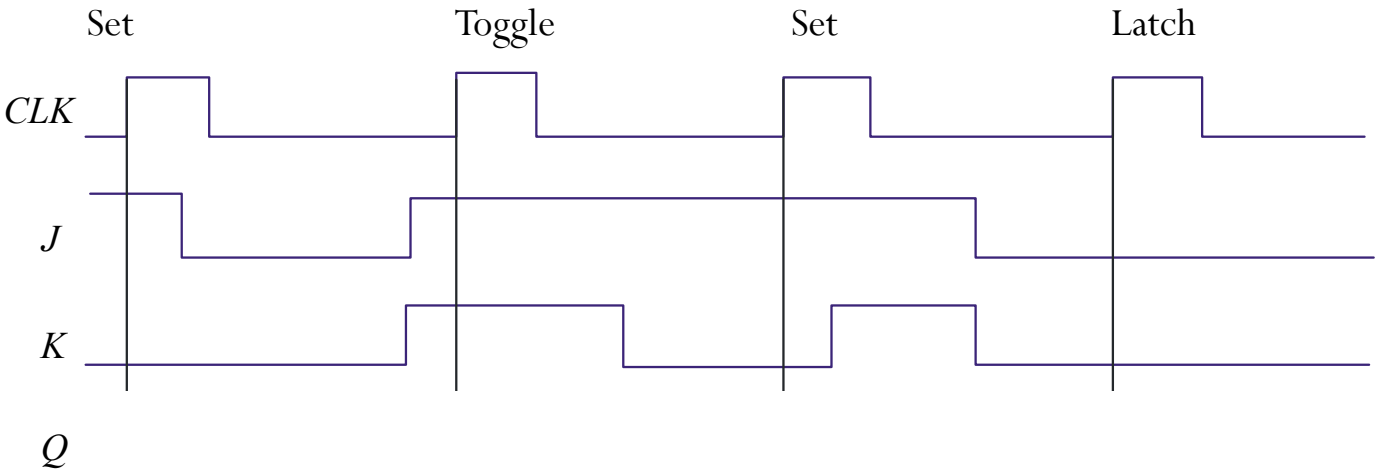




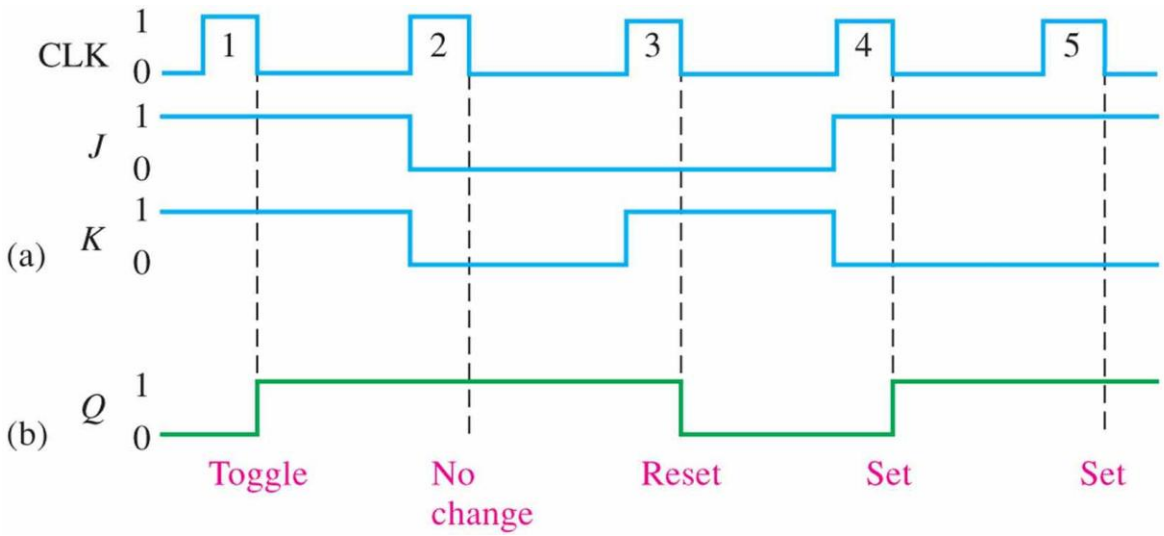
Exercise: J-K Flip-Flop

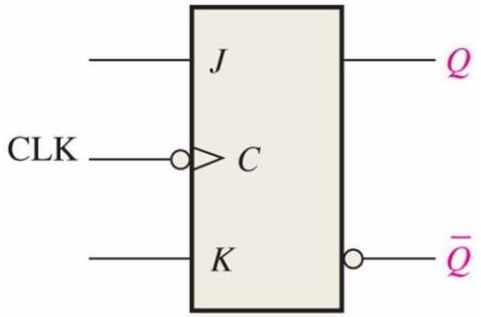


Inputs			Outputs		
J	K	CLK	Q	$\overline{Q}$	Comments
0	0	↑	Q_0	$\overline{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	$\overline{Q}_0$	Q_0	Toggle



Negative-Edge Triggered J-K FF



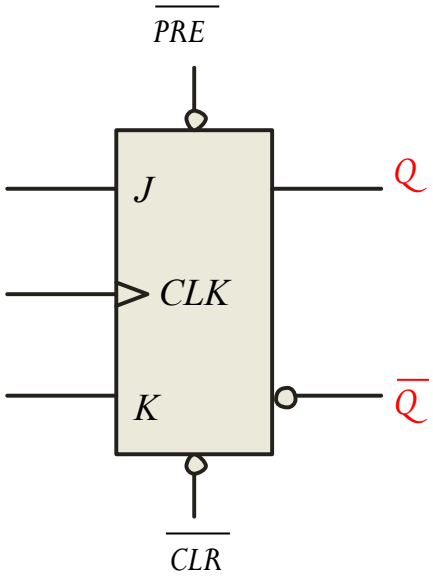


Caution

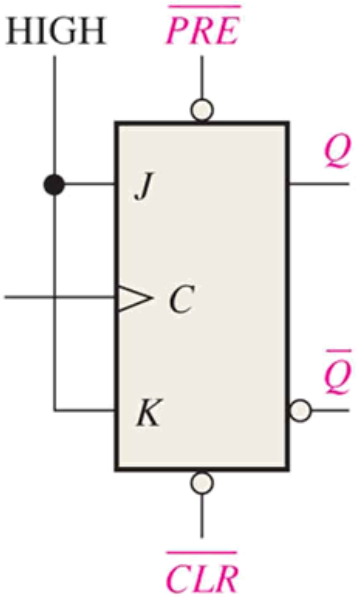
- When designing a circuit, do not change *input* values at the moment that the clock is rising.
  - This is the time that the flip-flops **read** the input values.

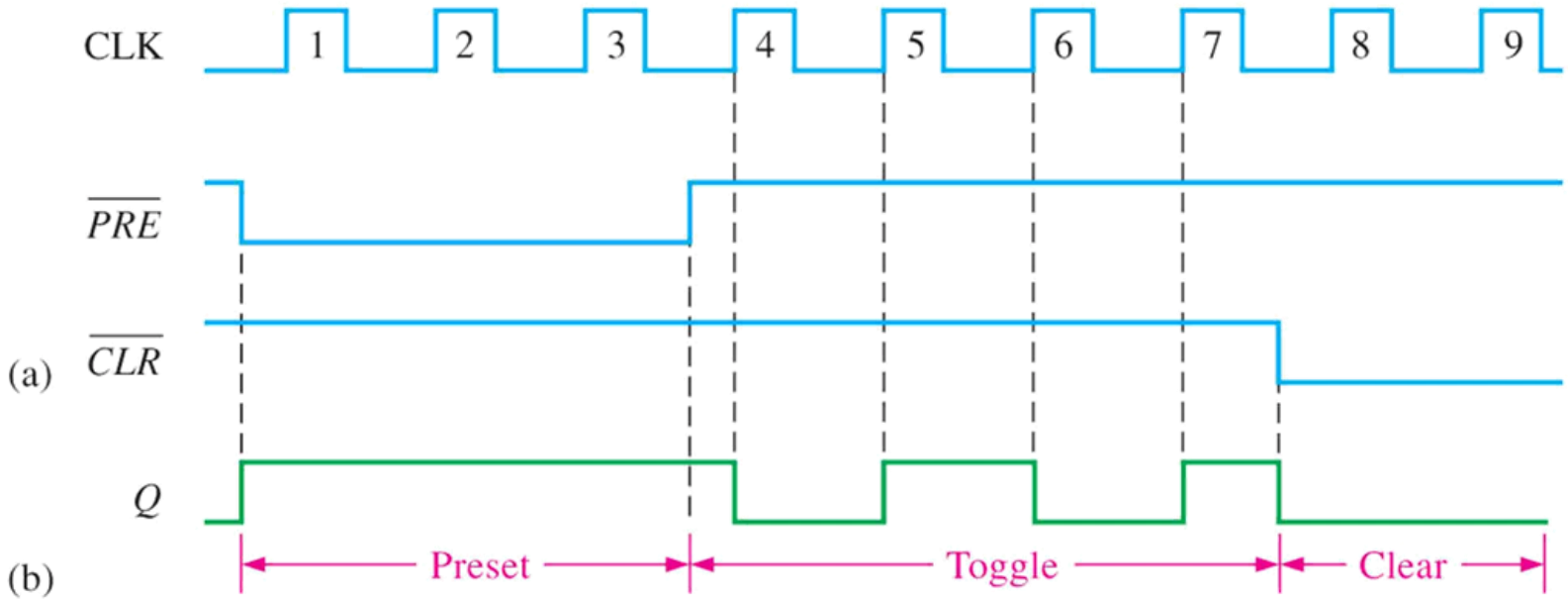
Asynchronous Inputs

- Most flip-flops have other inputs that are *asynchronous*, meaning they affect the output independent of the clock.
- Two such inputs are normally labeled **preset (PRE)** and **clear (CLR)**.
- These inputs are usually active-LOW.
- A J-K flip flop with active-LOW preset and CLR is shown.

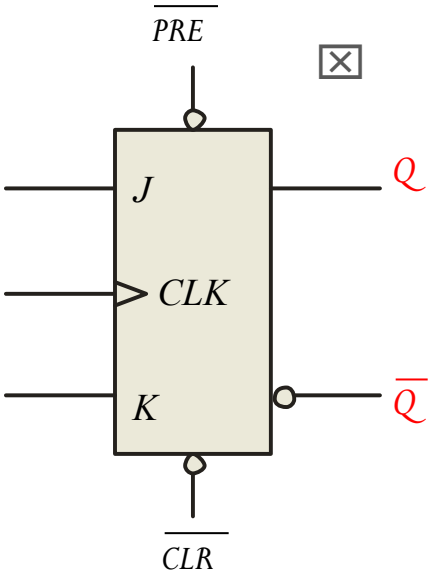


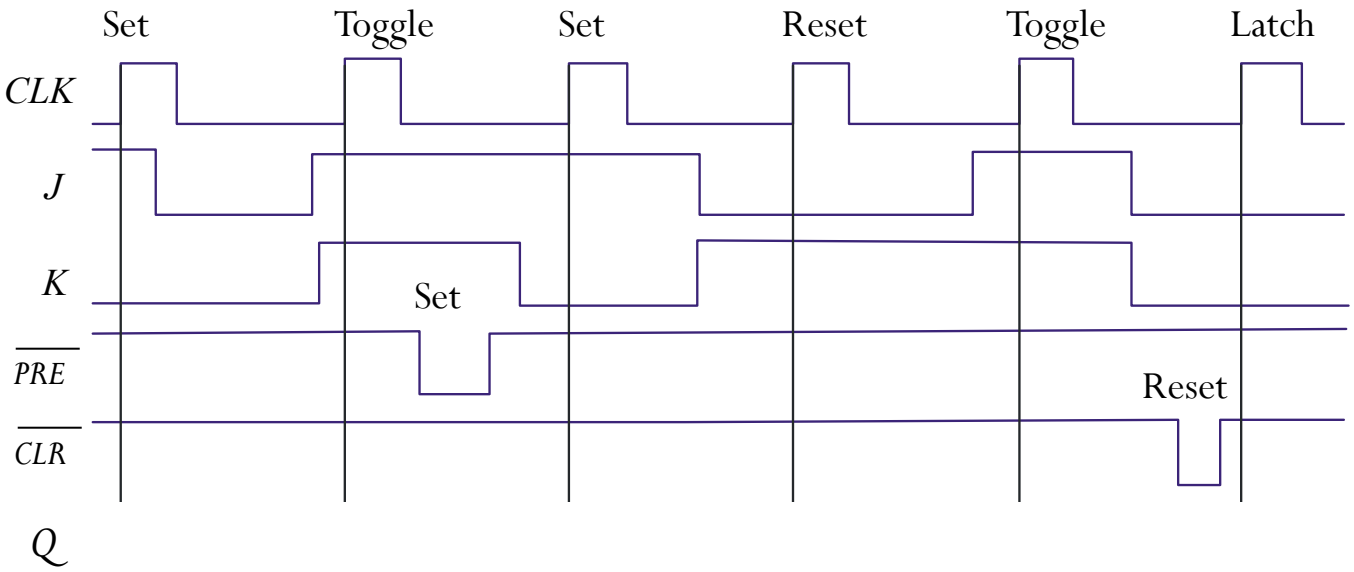
Example


HIGH
$\overline{PRE}$
Q
J
C
K
$\overline{Q}$
$\overline{CLR}$

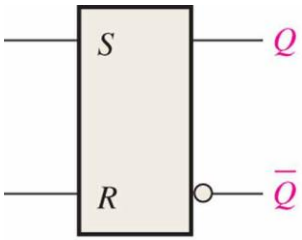

CLK
1
2
3
4
5
6
7
8
9
$\overline{PRE}$
$\overline{CLR}$
(a)
Q
(b)
Preset
Toggle
Clear

Exercise

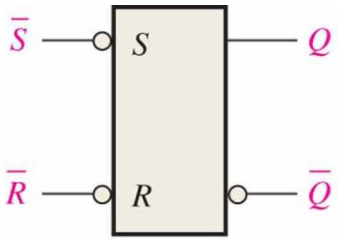

PRE
J
CLK
K
Q
Q
CLR


Set
Toggle
Set
Reset
Toggle
Latch
CLK
J
K
Set
PRE
Reset
CLR
Q

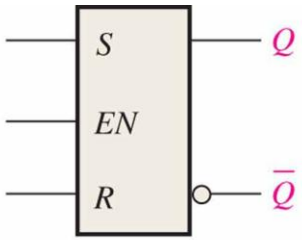
Logic Symbols: Latches and Flip-Flops



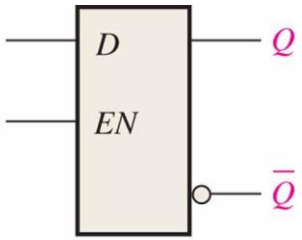
(a) Active-HIGH input S-R latch



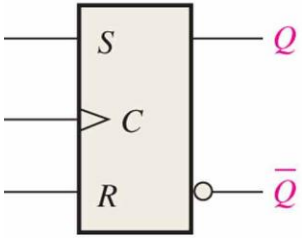
(b) Active-LOW input $\overline{S}$-$\overline{R}$ latch

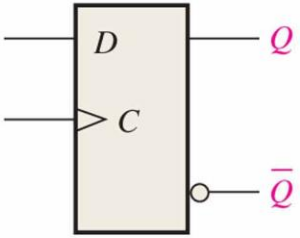


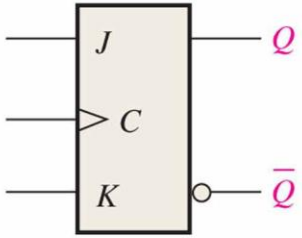
(c) Gated S-R latch

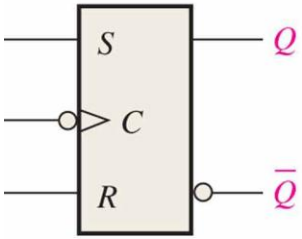


(d) Gated D latch

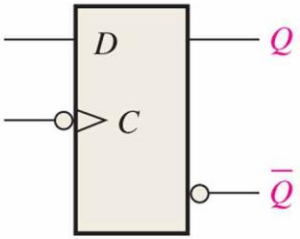




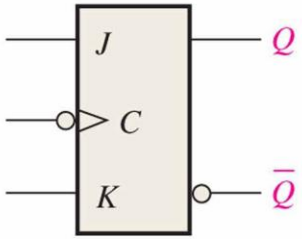




(e) S-R edge-triggered flip-flops



(f) D edge-triggered flip-flops



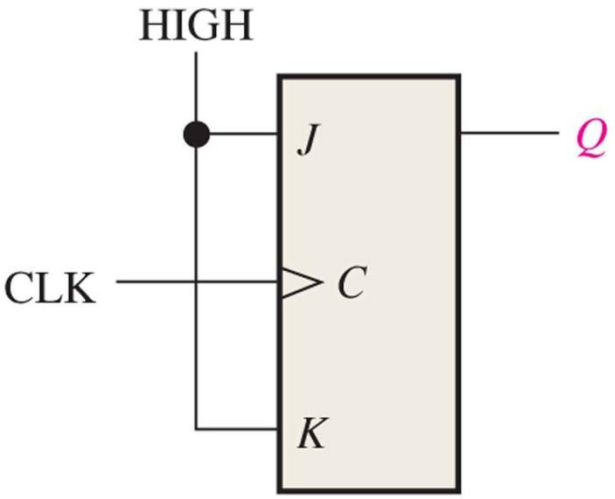
(g) J-K edge-triggered flip-flops

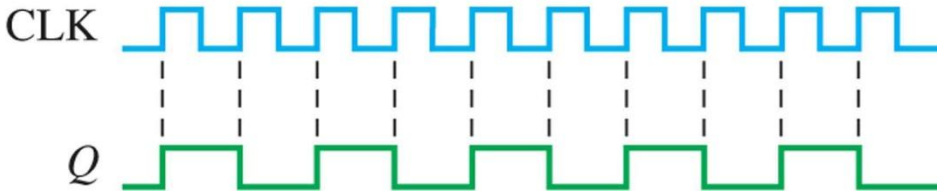
Latches and Flip-Flops

- The most basic storage elements are latches, from which flip-flops are usually constructed.
- Can maintain a binary state indefinitely (as long as power is delivered to the circuit), until directed by an input signal to switch states.
- The major differences among the various types of latches and flip-flops are the number of inputs the process and the manner in which the inputs affect the binary state.
- Although latches are most often used within flip-flops, they can also be used with more complex clocking methods to implement sequential circuits directly.
  - The design of such circuits is, however, beyond the scope of this class.

Some Applications

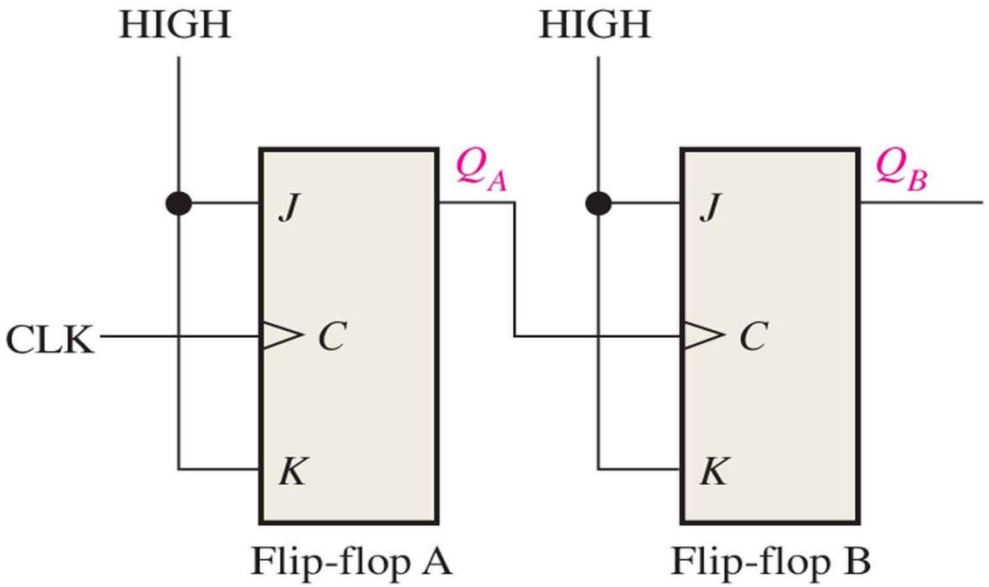
- Divide the clock frequency by 2

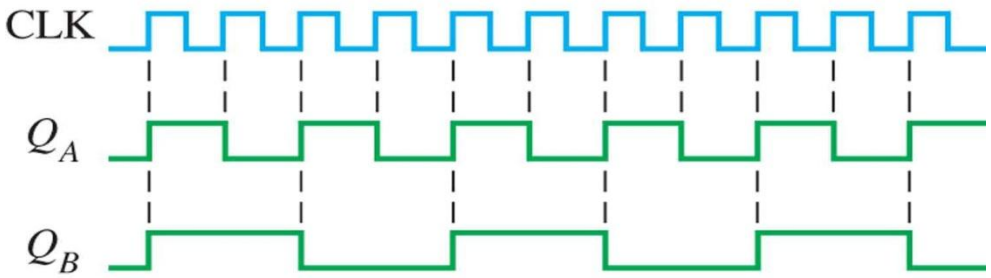




Some Applications

- Divide the clock frequency by 4





Time to take a look at your own exam

- Put all of your writing tools down (under table / in your bag).
- You have 5 minutes to look at your own exam.